



Floorplanning Principles

Richard Rodgers

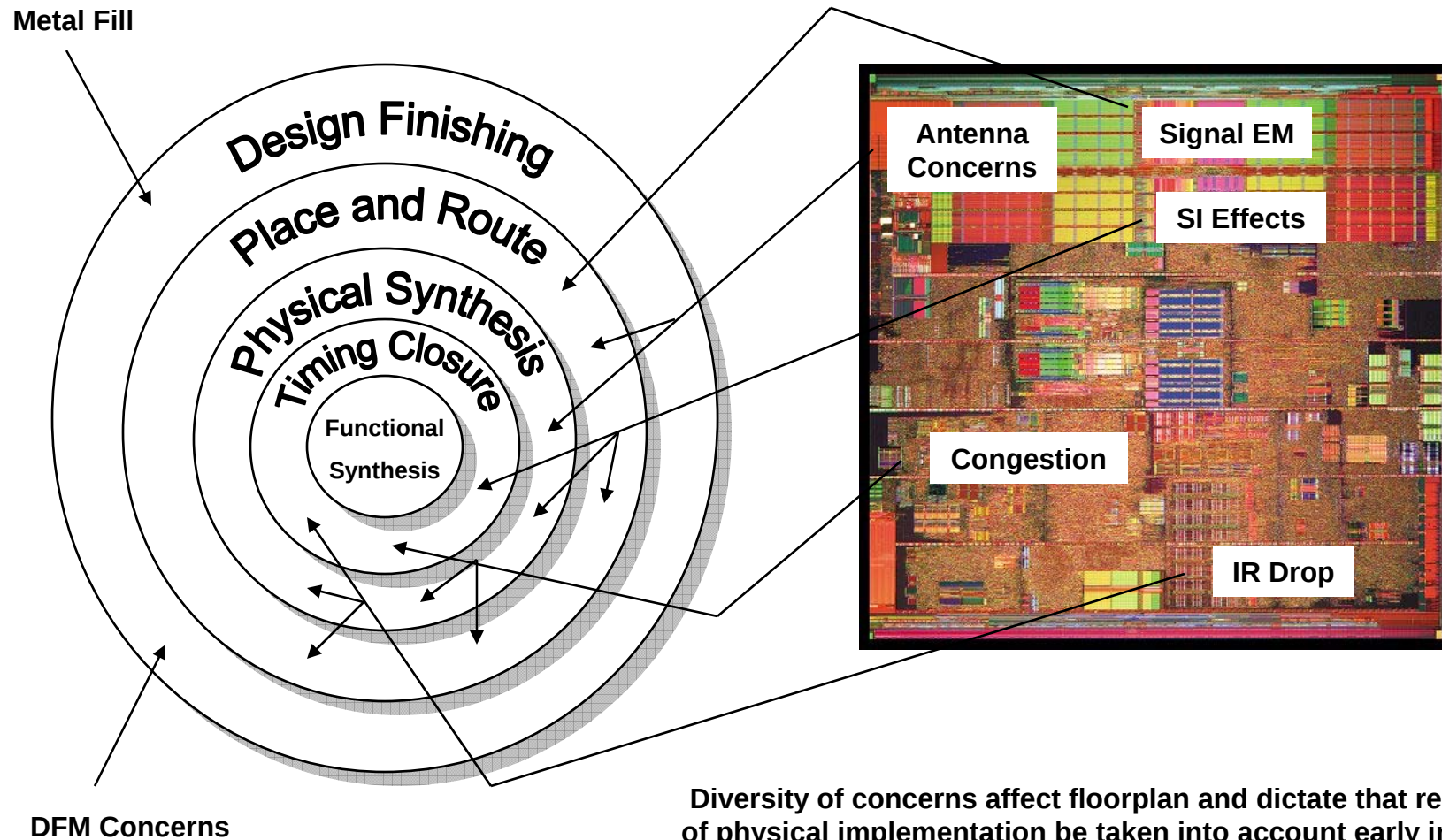
Agilent, APD

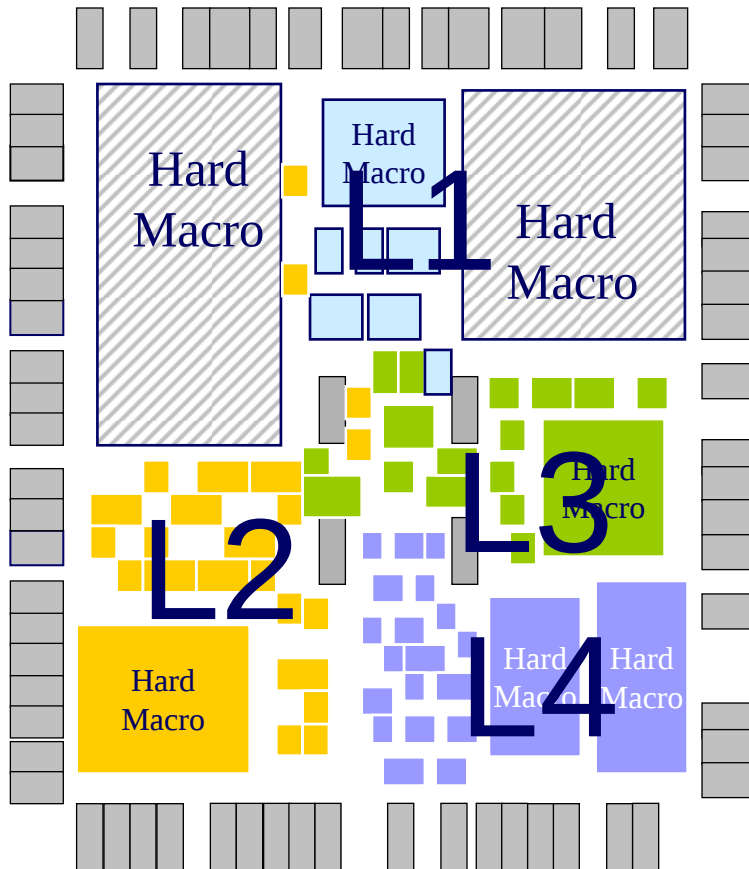
Kevin Knapp, Chris Smith

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Introduction – The Problem



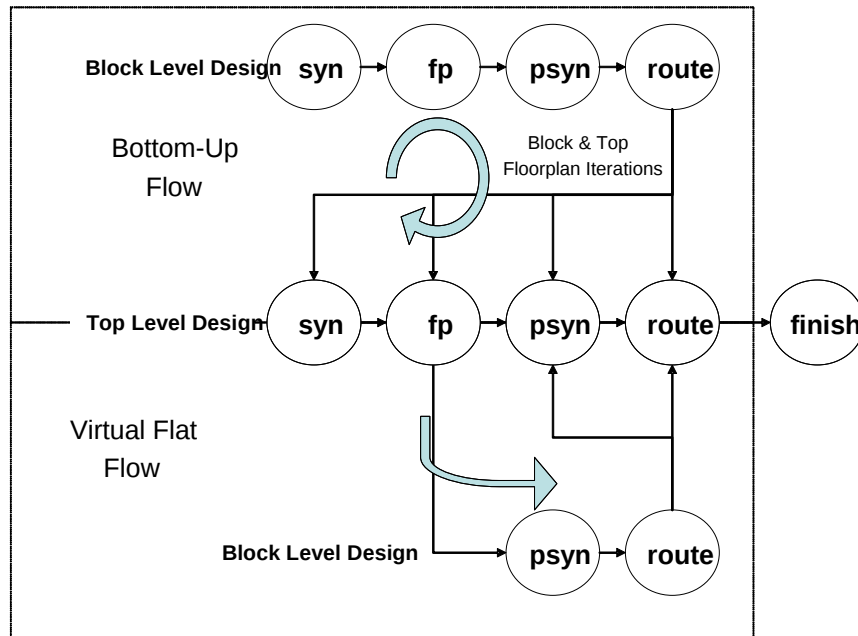


- Swift evolution of the design process
 - Floorplanning expertise thrust upon the well-balanced chip designer
 - Hierarchical design via divide-and-conquer of virtual flat flow
- Results in the need for:
 - Floorplanning best practices
 - Default methodology
- This presentation covers:
 - Guidelines and best practices for floorplanning 90nm designs
 - How they are used within an RTL2GDSII flow



- Hierarchical Design Flows
 - Bottom-up
 - Top-down (Virtual Flat)
- Power and Ground Insertion and Routing
 - Perimeter Power and Ground Rings
 - Standard Cell Power and Ground Straps
 - Power and Ground Trunks
 - IR Drop
 - > Timing Effects
 - > Assessment
 - Power Network Analysis
 - > IR Drop
 - > Electromigration
 - Power Network Synthesis
- Signal Integrity Concerns
 - Problems
 - Solutions
- Antenna concerns
 - Problems
 - Solutions
 - Special Considerations
- Additional Concerns
- Flowchart
- Conclusions

- Traditional Bottom-Up
 - Top level floorplan manipulates a collection of sub designs implemented in isolation
 - Only see simplified abstract of the sub-blocks at the top
 - Global level optimization cannot be performed
 - Blind to many of the concerns detailed earlier
 - Iterations on the sub-blocks may cause different top-level interactions resulting in delay of closure of the final floorplan
- Top-Down – Virtual Flat (VF)
 - Physical partitions determined by the floorplanner while having access to the complete netlist
 - Starts with top-level structural netlist and timing constraints
 - Floorplan, timing constraints, physical constraints generated for each sub-block (sub-blocks often referred to as “child” blocks)
 - Child block independently implemented and optimized all the way through place and route
 - Abstract representations are generated by the children for use at the top level
 - Hard macro IP may be instantiated in the top or child blocks



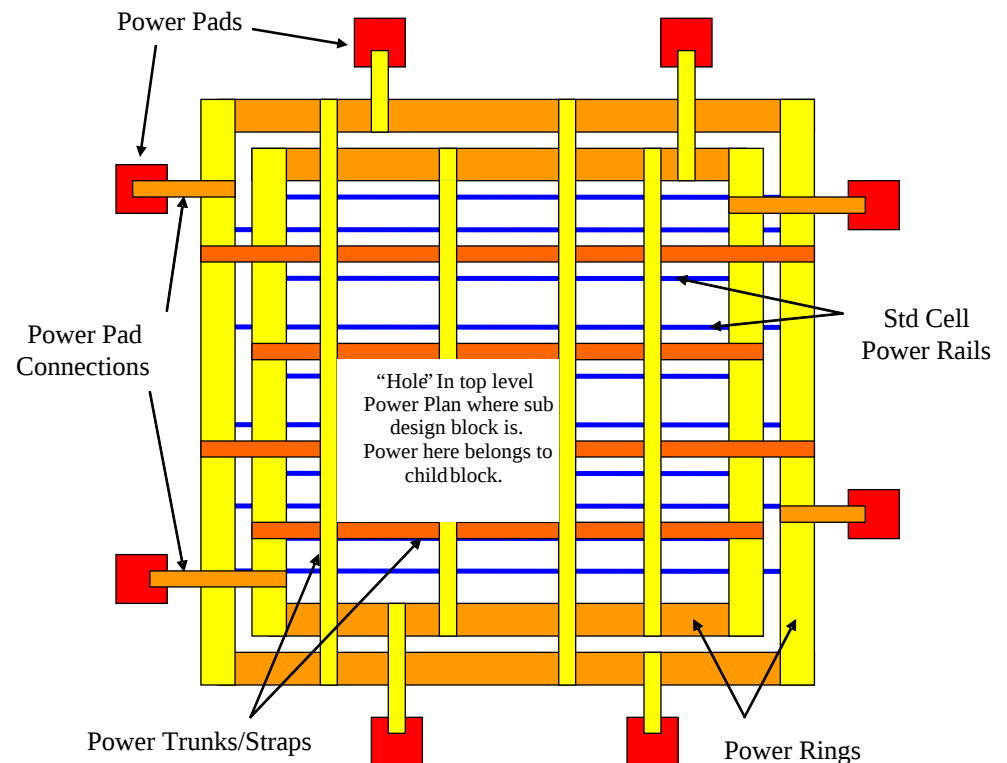
Key differences between Bottom-Up and Virtual Flat flows:

- Iterations between block and top floorplan for Bottom-Up (costly!)
- “Single pass” approach for Virtual Flat
 - The impacts of top level constraints and concerns known and fed forward in deterministic fashion. (much more efficient!)

Resolution of physical design concerns mentioned earlier may take different forms depending on whether the block being implemented is the top, child sub-block, or hard macro IP. This presentation will endeavor to account for these varying requirements.

Power and Ground Network – Definition of Terms

- An acceptable power and ground grid that distributes power to all cells with minimal voltage drop while consuming as little routing resources as possible is fundamental to a good floorplan
- Components include:
 - P/G pads for core and IO
 - Perimeter P/G rings around the core
 - P/G routing for standard cells – std. cell power rails
 - Horizontal and vertical straps and trunks across the core area
 - P/G perimeter ring for IO (not shown)



Perimeter Power and Ground Rings



- Assuming perimeter IO, power and ground rings should be placed around the perimeter of the standard cell core of the design
- Tools automate the insertion but user must set the size/width
- Sizing/width rule-of-thumb guidelines:
 - Assume each side of the chip carries $\frac{1}{4}$ of the power budget for the design
 - Use primary voltage of the core to convert the power into current
 - Use the max current density of the metal layer to determine the width
 - Typically use lower metal layers to ease connection to pads
 - If possible, limit line width to avoid the need for wide metal slotting

- Example:

Power budget for chip: 800mW

Routing layer for power rings: metal3 and metal4

Max current density for metal: 26mA/micron

Primary voltage of core: 1V

Width of perimeter P/G ring: $(800\text{mW}/4) = 200\text{mW}/\text{side}$

$$(200\text{mW}/\text{side}) / 1\text{V} = 200\text{mA}/\text{side}$$

$$(200\text{mA}/\text{side}) \times (1\text{micron}/26\text{mA}) = 7.69\text{micron}/\text{side}$$

Use 8micron/side for margin.

Hard Macro IP Perimeter Power Rings



- Best to create perimeter rings around hard macro IP
 - Orientation independence
 - VF flow will result in perimeter ring be placed at the level of hierarchy in which the hard macro is instantiated
 - Use the same rule of thumb for size as described for the top level
 - Floorplanning tool automates the connection to the power rings/trunks



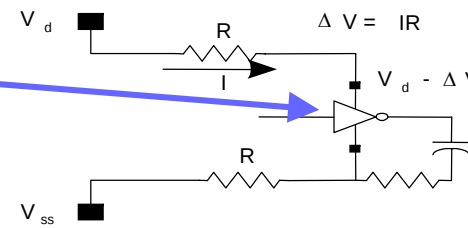
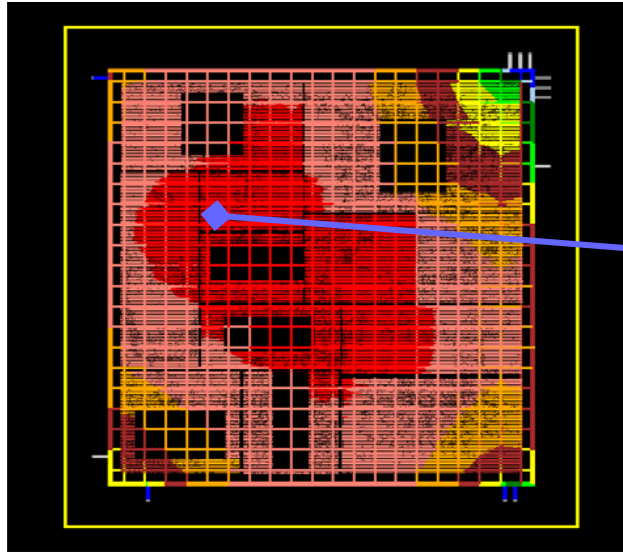
Standard Cell Power Rails



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- Continuity of standard cell power and ground may be accomplished by abutment of cells and insertion of filler cells.
- However, explicit routing of standard cell power and ground should be done as a fail-safe measure to ensure:
 - Continuity of power and ground rails
 - Distribution of power and ground to every usable placement site
 - Connection of the standard cell P/G to the perimeter rings
- Floorplanner automates the insertion. User must specify width.
 - Rule-of-thumb:
 - Use twice the width of the straps contained within the cells
 - Use lowest horizontal metal layer

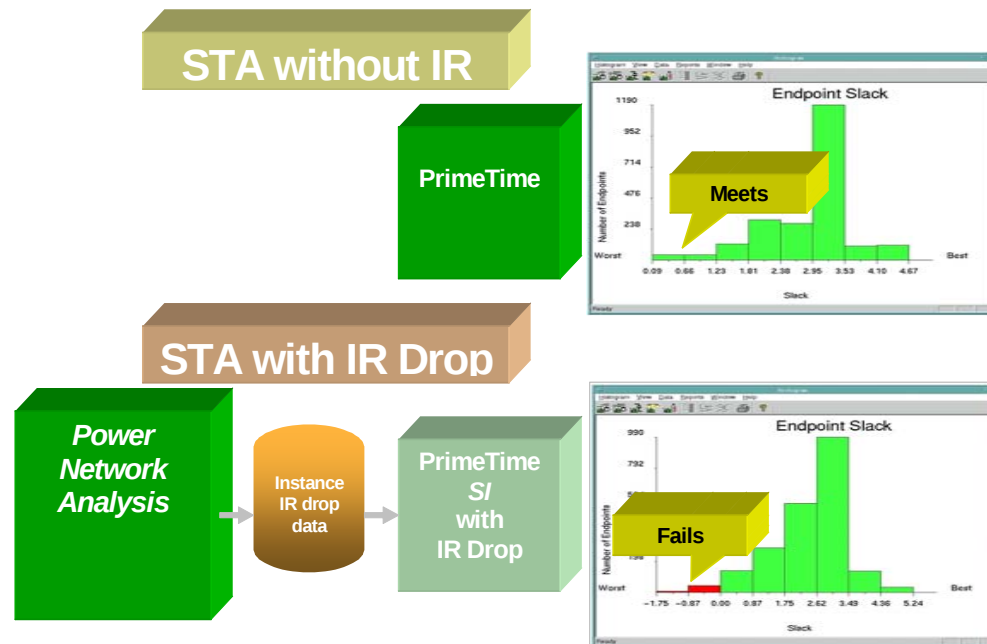
- Additional power and ground connections are needed to adequately distribute power and minimize the voltage drop across the P/G network
- Additional P/G trunks represent the dominant factor in controlling IR drop and electromigration
 - Components of perimeter rings are “rule-of-thumb” as are standard cell power rails
 - Greatest degree of freedom exists in size, location and number of P/G trunks
- Note that no special consideration need be given to child soft-macro blocks while establishing the power grid at the top level. The Virtual Flat flow will push the power structure of the region assigned to the child into the child block itself.



- Resistive routing from power pad to cell power pin results in reduction of supply voltage
- Instance specific IR drop depends on the current that the power network must deliver to the area to support targeted frequency/cell switching
- Therefore, IR drop varies across the design.
- Must place addition P/G trunks to mitigate the voltage drop



IR Drop – Timing Effects



- Cell delay is function of supply voltage
- Instance-specific IR drop of P/G network degrades cell performance, risks timing failure
- Endpoints with minimal margin are at highest risk

How do we assess and address IR drop?



IR Drop Assessment



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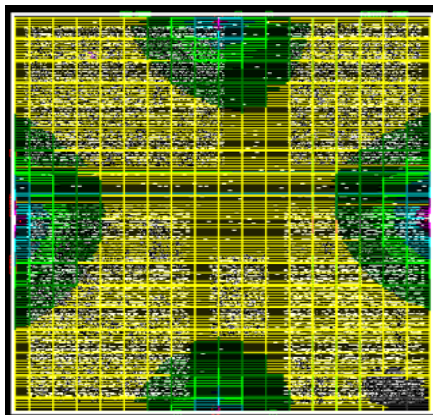
- Historically IR drop has been assessed after final place and route
 - Risks iteration all the way back to floorplanning
 - Iterative, time-consuming resolution
 - P/G network often over-designed as a result
 - Risks congestion and routability problems
- Current floorplanners capable of Power Network Analysis (PNA) to assess IR drop
 - Gives visibility very early in the flow
 - Fast run times
 - Not as accurate, but **correlation is the key!**
 - Jupiter XT within 15-20% of sign-off AstroRail analysis

Power Network Analysis – IR Drop

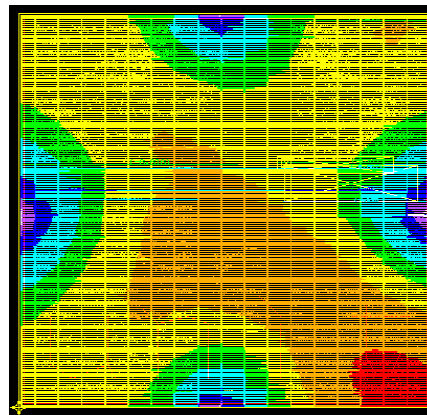


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PNA (design planning stage) Astro Rail (signoff)



Worst Case IR drop < 7 mV



Worst Case IR drop < 9 mV

- Heat map type of display
- General contour correlates very well
- Absolute values enable progression through design flow with confidence

- Accurate PNA for best correlation requires:
 - Complete PG network – rings, rails, trunks
 - DRC-clean PG network
 - Prototype or global route for accurate assessment of load
 - Accurate switching information



Power Network Analysis - Electromigration

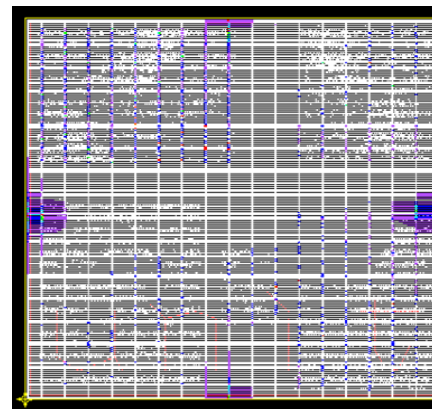
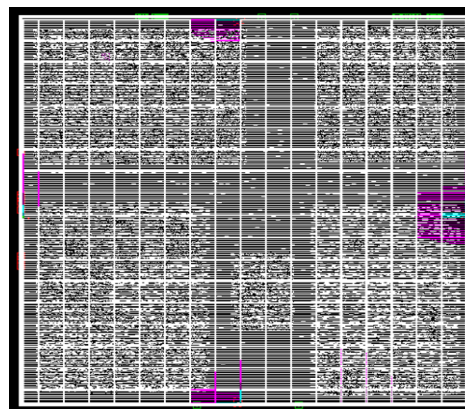


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- Electromigration problems result from excessive current density over time
 - Performance degradation via resistive shorts
 - Catastrophic failure due to open or short circuit
- Also a function of size, number and location of PG trunks
- Correlation between floorplanner and AstroRail not as good as for IR drop
 - AstroRail considers larger set of design rules
 - Trade accuracy for run time given development stage of design

PNA (design planning stage)

Astro Rail (sign-off)



•0.790mA/um (M7)
•3.346mA/um (M8)

Worst Case EM

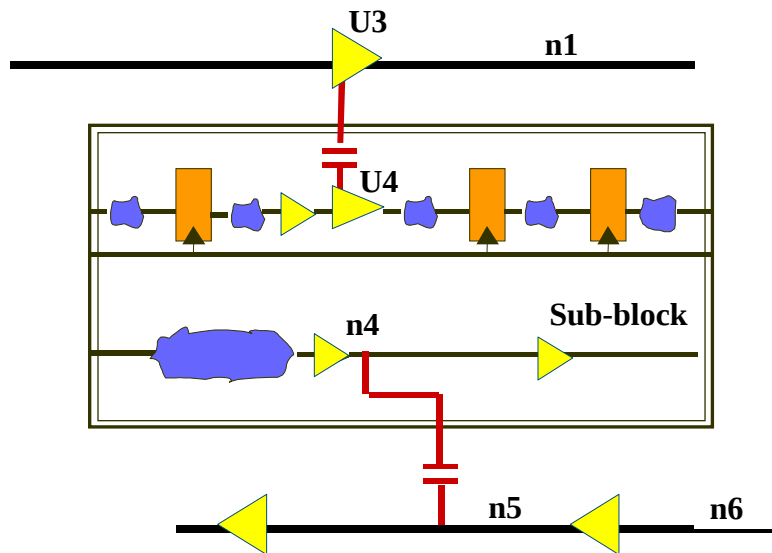
•1.05 mA/um (M7)
•4.22 mA/um (M8)

How Many Trunks are Enough?



- When IR drop and electromigration meet targets
 - But this is iterative and time consuming
- Jupiter XT offers Power Network Synthesis (PNS)
 - Accepts one or all of basic constraints: max IR drop, max number of trunks/straps, min metal width, metal layers to use
 - Performs PNA under the hood. If acceptable, commit the results. If not, refine constraints.
 - Can be run on a specific region of the design
 - Full PNS or sizing of an existing network to meet constraints

Signal Integrity Concerns - Example



- Signal integrity issues result in two primary failure modes:
 - Timing failures – cross talk between nets can decrease or increase the delay depending on whether the victim and aggressor are switching in the same or different direction
 - Functional failures – noise coupling between nets and/or cells can induce glitches that result in unintended logic transitions

Cross-talk between long, parallel routes n4 and n5 may result in a timing failure.



Solution = eliminate long parallel routes

Noise coupling between instances U3 and U4 may result in a functional glitch failure.



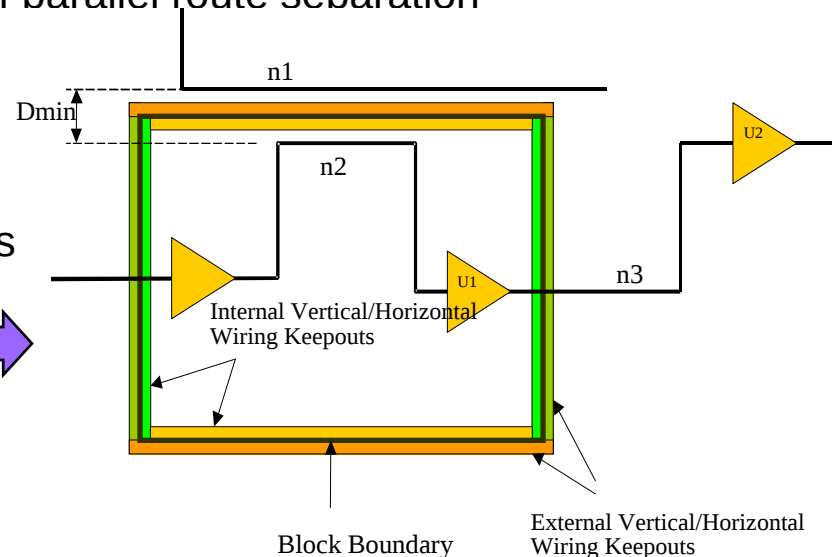
Solution = provide placement separation for cells in differing levels of the hierarchy

- The problem:
 - No detailed visibility into top level route or placement when implementing a child block.
 - Similarly for top level – no visibility into child block when performing top level routing.
 - This problem manifests itself both in the horizontal and vertical planes.
- The solution:
 - Horizontal plane:
 - Wiring and placement halos around perimeter of the block
 - Supplement the above by limiting max routing length at top level
 - Vertical plane:
 - Minimize non-preferred routing for over-the-block routes
 - Establish shielded channels for through-the-block routes

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- Result:

- n_1 and n_2 are 16 to 22 tracks apart
- Length of n_3 is known and bounded





Signal Integrity Concerns: Horizontal Plane Solution – Some Hints



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- Hint1 - Wrong-way routing
 - Astro can perform routing in non-preferred direction
 - Thus, halo is not fool-proof
 - Need the following to minimize wrong-way routes
`axSetIntParam droute wrongWayExtraCost 50`
- Hint 2 – Alternative to halo
 - Remove cross-hierarchy cross-coupling by creating a ground ring around the outside of the macro block.
 - Couples the potential internal and external long, parallel routes to ground rather than to each other.
 - May result in smaller overall block area
 - Best for small blocks



Signal Integrity Concerns: Vertical Plane Solution



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- Long parallel routes in metal layers above those used inside the sub-block must also be eliminated. Three possibilities:
 - No routing is allowed over the sub-block – no issue.
 - Over-the-block routing is allowed in layers not utilized by the sub-block
 - Typically not a problem since vertically adjacent layers are typically orthogonal
 - Use axSetIntParam as described earlier to minimize wrong-way routing
 - Through-the-block routing is allowed
 - Establish pre-determined channels through the block.
 - **Reserve all the routing resources in the channel via wiring keepouts**
 - **Shield the channel with ground straps to prevent cross-coupling**



Signal Integrity Concerns: Hard Macro IP Tips



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- The designer of hard macro IP does not know the context the IP block will be used in.
- Must include entirety of halo, or shielding, for cross-hierarchy cross-coupling mitigation within the bounds of the hard macro IP block.
- Similarly for the user of hard macro IP – the user does not know the contents and physical proximity of objects inside the hard macro IP block.
- Must include entirety of halo, or shielding, outside of the bounds of the hard macro IP block.



Antenna Concerns: The Problem



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- The problem – similar to cross-hierarchy cross-coupling concerns for signal integrity:
 - No detailed visibility into top level route when implementing a child block.
 - Similarly for top level – no visibility into child block when performing top level routing.
 - Thus, additional routing at the other hierarchical level may push the net over the threshold for process antennas.



Antenna Concerns: The Solution



- The Solution
 - Not a problem if both blocks use Astro.
 - Astro can annotate the physical model of the child block with information regarding routing inside of the block on its top level nets.
 - Astro can then fix/avoid antenna issues for these top level nets during top level route.
 - Otherwise, when implementing hard macro IP or soft macro child blocks:
 - Antenna prevention diodes are required
 - Jupiter can place the diodes in proximity to the top level ports.
 - **User can specify all inputs, outputs or bidirs**
 - **Don't forget to mark the diode cells as fixed placed**
 - **Recommend diodes be placed within 20um of the port**
 - Diodes are connected in Astro
 - Similar strategies have been developed in PhysicalCompiler



Antenna Concerns: Special Considerations



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- When using hard macro IP
 - Internal structures of IP may pose an antenna problem. Therefore insert antenna protection diodes at the exterior of the macro in close proximity to the pins.
- Consistent rules across tools
 - Jupiter, Astro and Hercules offer different rules for antennas:
 - Allowable signal routing area as a multiple of minimum geometry transistor gate area
 - Can be for a given routing layer or cumulative for the net
 - Be sure the same rule is specified across the tools (tech file and Hercules run deck).
- Handling of diodes throughout the flow
 - Many libraries do not have CLF files for diode cells. Therefore, may need to exclude diodes from Verilog netlist out of Astro used for Hercules LVS.
 - Best to include diodes in netlist and RC extraction for STA. May therefore need a second netlist out of Astro.

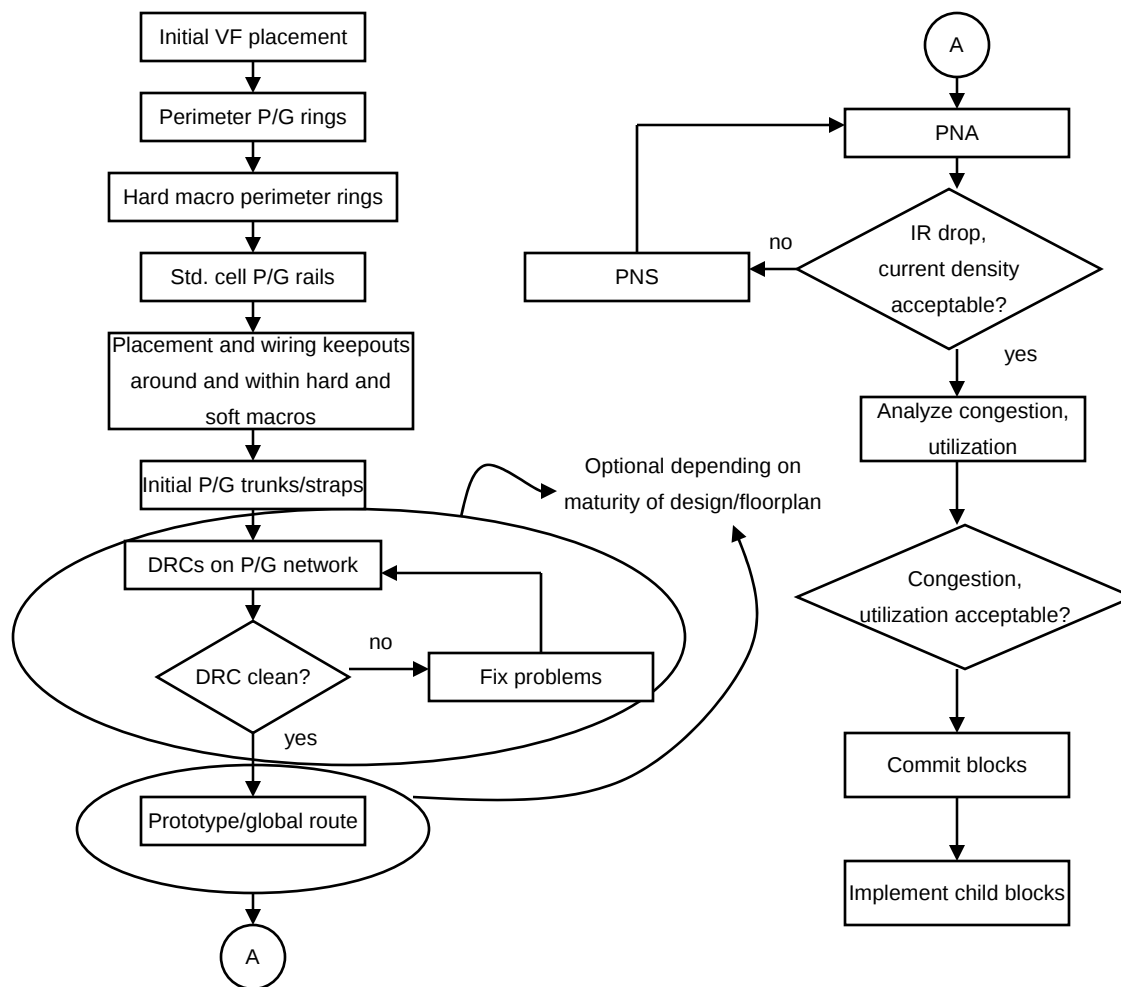


- Child soft macros and hard macro IP
 - Placement halo recommended around interior of block
 - Mitigates noise coupling and possibility of noise glitch functional failures across the hierarchy
 - Avoids DRC failures around the perimeter of the block across the hierarchy
 - Frees up routing resources around the perimeter to ease access to the top level pins of the macro
- Top level – Once all the above concerns have been addressed:
 - Perform final VF placement, power network DRCs, prototype/global route, and PNA
 - Final congestion and utilization analysis
 - No congestion hot spots
 - Child block 65% utilization max.

- Silicon Results at Agilent
 - 3 90nm designs successfully implemented with this methodology
 - Working silicon turned-on and characterized.
 - Critical path registered timing paths running at 850 MHz.

- Conclusions
 - Knowledge of the physical implementation of the design early in the design flow is imperative for timely design implementation.
 - 90nm SOC design presents new/magnified concerns for physical design.
 - With proper attention these concerns can be adequately handled early in the design flow via attentive floorplanning and the VF flow.
 - Standardization of methodologies assists in timely development and efficient resource utilization.
- Future Work
 - Expound on the detail of the topics contained herein:
 - Capture detail in checklist traveler to aid in comprehensive attention. (Reference the checklist in the appendix of the paper.)
 - Implement details, where possible, into an automated floorplanning system.

Simple Flowchart



- This flowchart is only intended to roughly capture the relative order of the topics represented in this presentation and the associated paper. There are MANY floorplanning details not represented here.
- There are various analysis steps intermingled with the tasks represented here (e.g. congestion, timing)
- This flowchart represents one potential ordering. Even these task could be ordered differently; yet it does give some idea of dependencies and order of operations.